

FIG. 1
Conventional Art

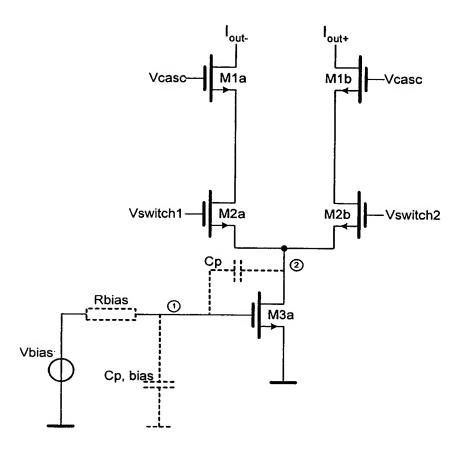


FIG. 2 Conventional Art

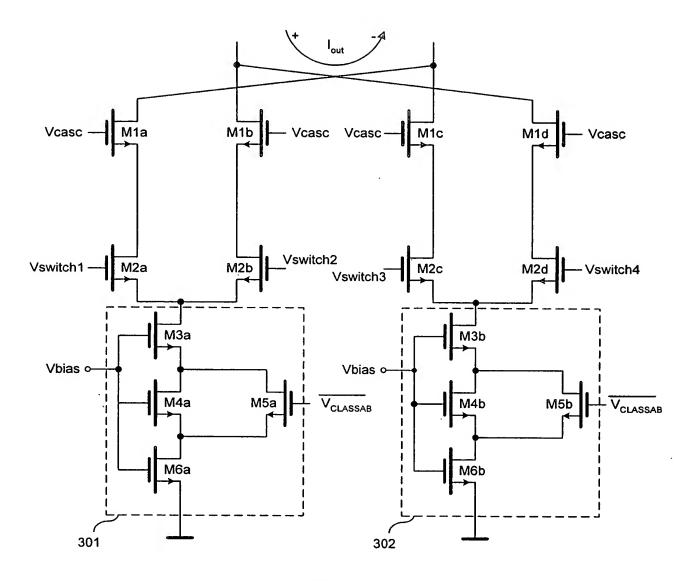


FIG. 3

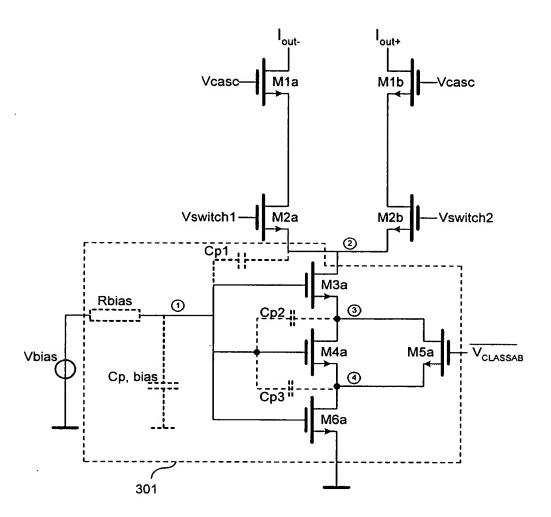
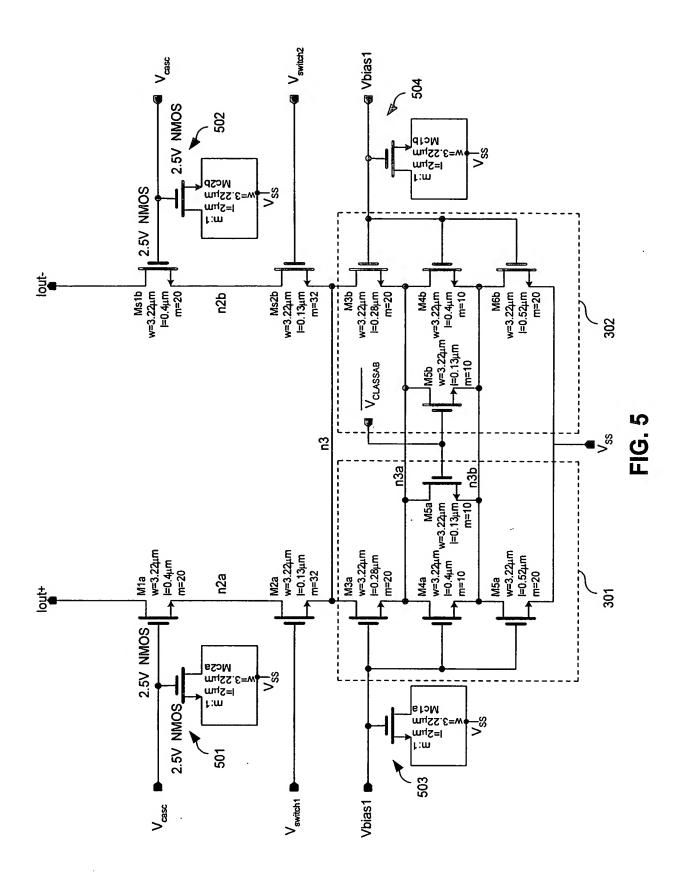


FIG. 4



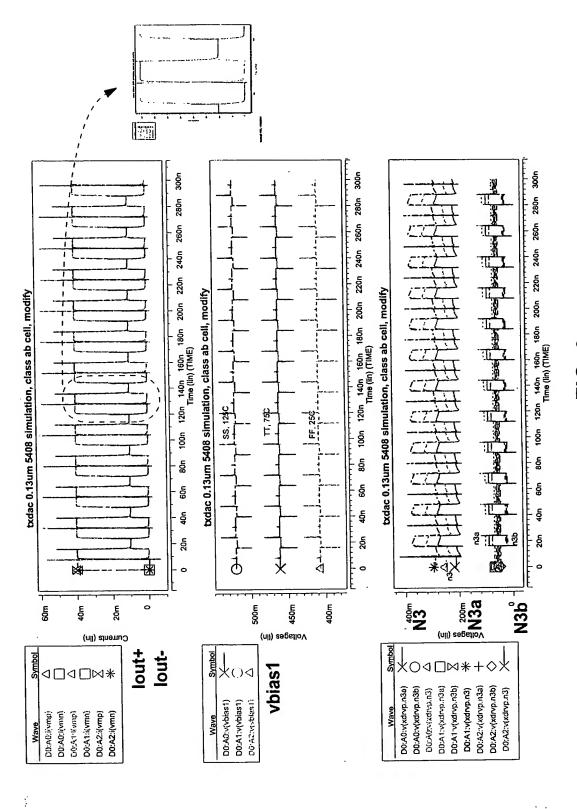
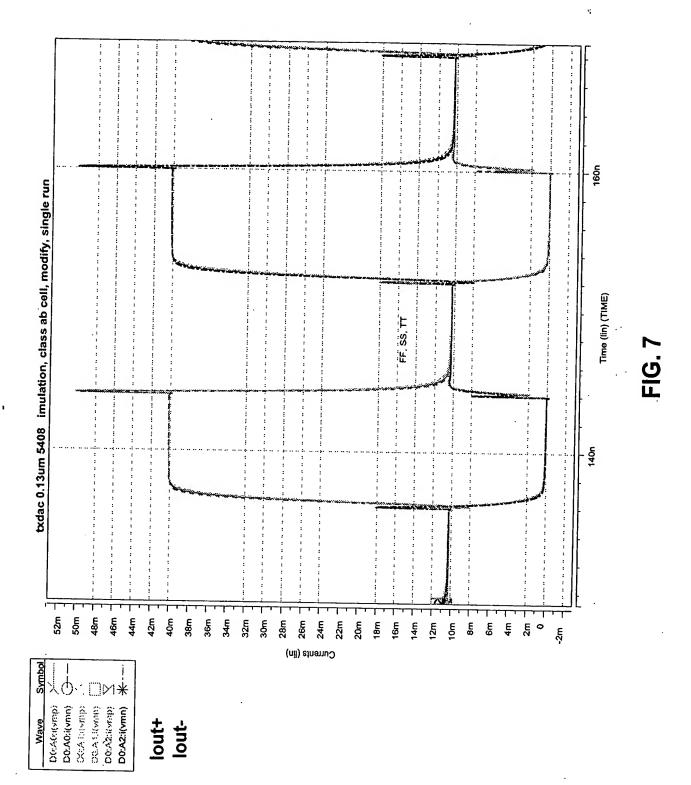
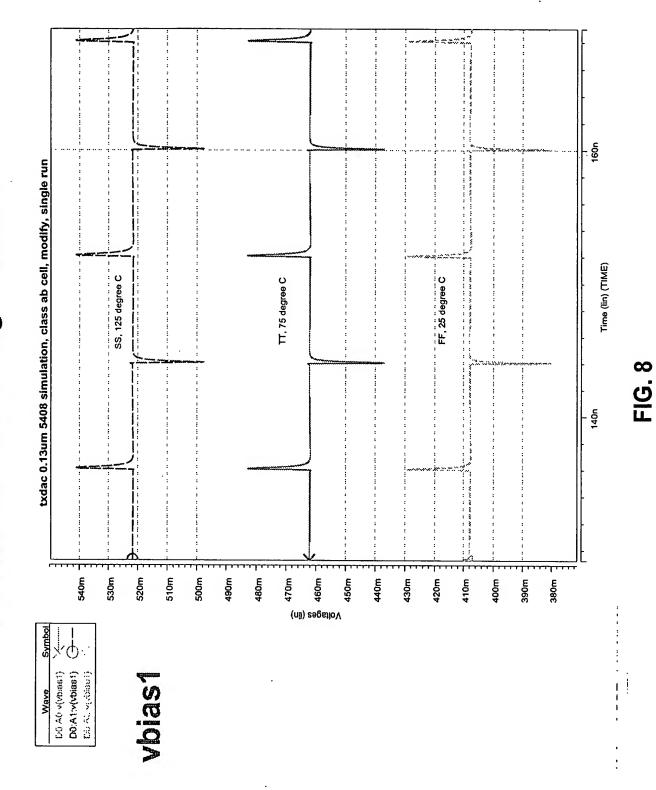


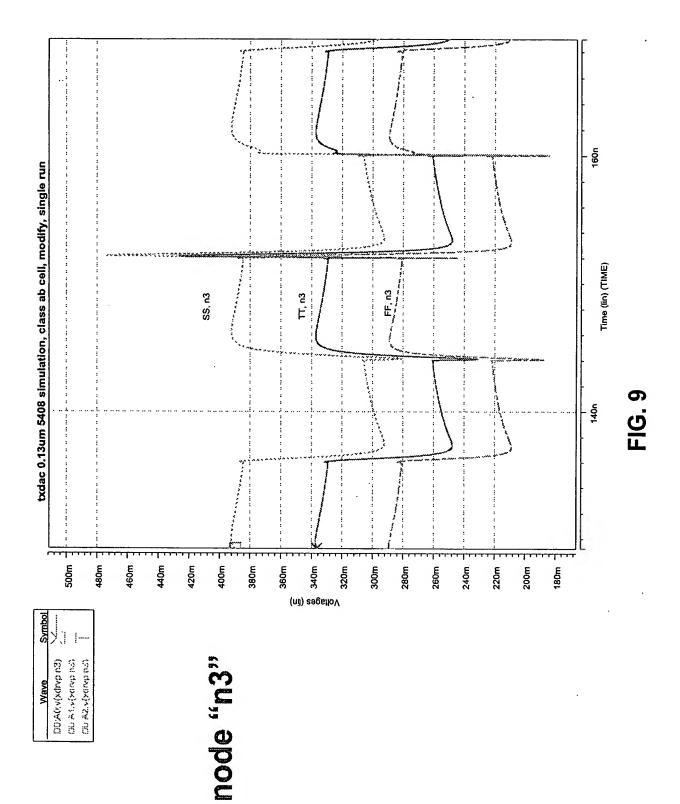
FIG. 6



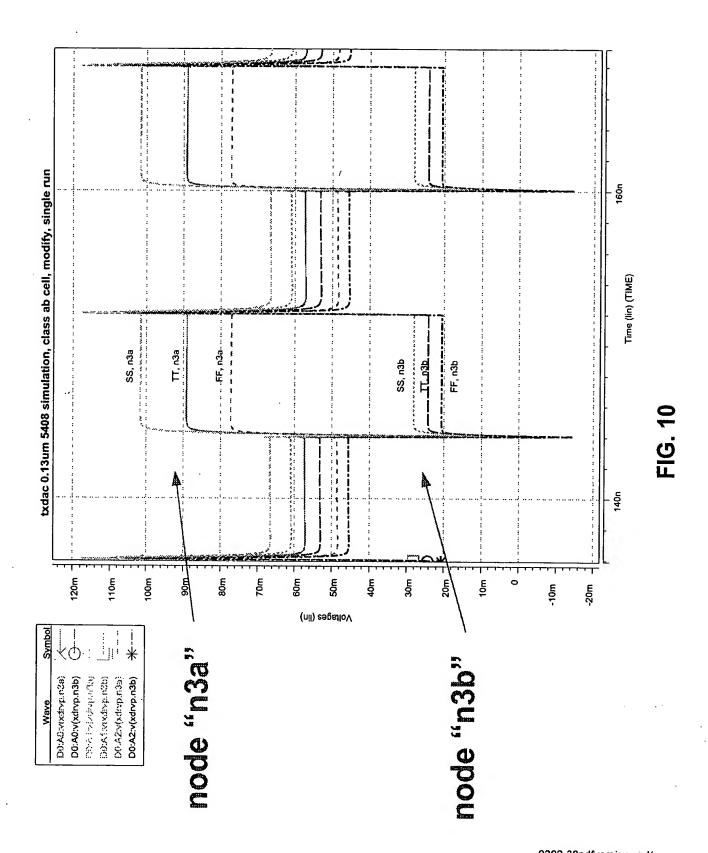
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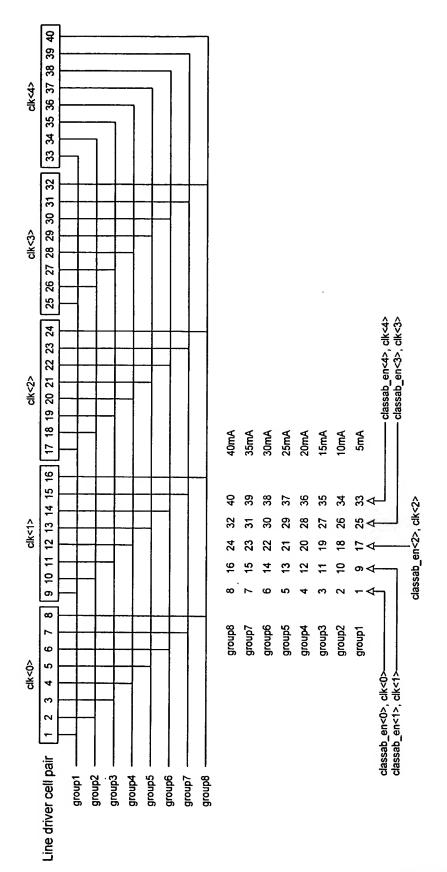
Simulated node voltage "vbias1"





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